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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/537,669	03/29/2000	Takeshi Yamamoto	P107317-00003	5975

7590 02/10/2005

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EXAMINER	
AGGARWAL, YOGESH K	
ART UNIT	**PAPER NUMBER**
2615	

DATE MAILED: 02/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/537,669	YAMAMOTO, TAKESHI	
	Examiner	Art Unit	
	Yogesh K Aggarwal	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 10-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 10-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 March 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11/05/2004 has been entered.

Response to Arguments

2. Applicant's arguments filed 09/08/2004 have been fully considered but they are not persuasive.

Examiner's response:

3. Applicant argues with respect to claim 1 and 10 that Pape et al. fails to disclose or suggest a second field that stores the position data of a defective pixel. The Examiner disagrees. Pape et al. clearly teaches that a digital representation of the dark current of each pixel 14 (defective pixel) is stored in the frame buffer 16 at addresses corresponding to the location (second field) of each pixel 14 in the CID array 12 (col. 3 lines 42-46). Pape also teaches when the CID 12 is subsequently exposed to incident scene light, pixel data (image data) from the CID is input to the frame buffer 16 (memory) on a pixel by pixel basis for each corresponding location (first field) therein (col. 3 lines 46-49). Therefore Pape et al. teach the recited limitations of claim 1 "a memory having a first field for storing image data of one frame and a second field for storing position data of a defective pixel of the image sensor".

4. Applicant argues (claims 1 and 10) that Katoh merely teaches that the corrected image data replaces the defective data in the data sequence being delayed, showing that the delay circuit either provides the delayed data or provides the corrected data, rather than the corrected data for each pixel being outputted while the delayed image data is also being outputted. The Examiner respectfully disagrees. As noted in the previous office action the claim is broad and only recites a second output for supplying each of the corrected image data. The defect correction circuit 107 disclosed by Katoh in col. 5 lines 24-29, figure 6 for forming corrected image data checks the threshold level of each pixel (col. 4 lines 31-36) and the pixel for which the signal level exceeds the threshold level is stored in the memory. Therefore in response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e. defect correction circuit 2 calculates correction data for all the pixels irrespective of whether or not there is a defective pixel, See Page 8 lines 14-16 of the Specification) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993)]. Therefore the argument is not relevant.

DETAILED ACTION

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 2, 4, 7, 8, 10, 12, 13, 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Katoh et al. (US Patent # 5,796,430) in view of Pape et al. (US Patent # 5,047,863).

[Claim 1]

Katoh teaches an image processing apparatus for processing image data supplied from an image sensor (figure 1), comprising

A delay circuit (figure 7: 702) having a first input for receiving image data sequentially supplied from the image sensor, a first function circuit for delaying the received image data by a time required for defect correction process, and a first output for supplying each of the delayed image data (col. 5 lines 39-52, figures 7, 8A-8D).

a counter (figure 5: 501, 502) for counting the number of pixels of image data sequentially transferred from the image sensor (col. 4 lines 37-53).

a defect correction circuit (figure 1: 107) having a second input for receiving the image data supplied from the image sensor, a second function circuit for forming corrected image data for each pixel based on image data of pixels adjacent to a pixel of interest and a second output for supplying each of the corrected image data (col. 5 lines 24-29, figure 6)[The Examiner notes that the defect correction circuit 107 disclosed by Katoh in col. 5 lines 24-29, figure 6 for forming corrected image data checks the threshold level of each pixel (col. 4 lines 31-36) and the pixel for which the signal level exceeds the threshold level is stored in the memory. Therefore in response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e. defect correction circuit 2

calculates correction data for all the pixels irrespective of whether or not there is a defective pixel, See Page 8 lines 14-16 of the Specification) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993)].

Katoh further teaches a control means (figure 1: 103 for generating CK1 shown in figure 7) for writing the image data supplied from the second output of said defect correction circuit in the first field of said memory at a storage location corresponding to the defect pixel, if a count of said counter becomes coincident with a number corresponding to the position data of the defective pixel in the second field of a memory (col. 5 lines 14-18). Figures 7 and 8A-8D disclose that the image data supplied from the delay circuit which is not defective (e.g. A.sub.11) must be stored in the same memory 110, if the count is not coincident with the number corresponding to the position data of the defective pixel. Katoh does not explicitly teach a memory wherein a memory having a first field for storing image data of one frame and a second field for storing position data of a defective pixel of the image sensor. However Pape et al. teaches that this limitation is well known and used in the art (col. 3 lines 43-49, figure 1: 16). Therefore taking the combined teachings of Katoh and Pape, it would have been obvious to one skilled in the art at the time of the invention to have been motivated to incorporate a memory wherein a memory having a first field for storing image data of one frame and a second field for storing position data of a defective pixel of the image sensor into the image processing circuit of Katoh as taught by Pape. The benefit of doing so would be that same memory can used for

storing image data as well as position information of defective pixels leading to a cost saving in terms of die area.

[Claim 2]

Pape teaches a storage location in said memory (figure 1: 16) is identified by a row address and a column address, the first field stores the image data of each line at a corresponding row address, and the second field stores the position data of the defective pixel at the same row address" reads on Pape (col. 4 lines 30-46). [Lines 30-38 show that if the dark pixel does not exceed the threshold i.e. if it is a good pixel then it is stored in the frame buffer 16 by the write pulse. Lines 39-46 show that if the dark pixel data exceeds a threshold i.e. for a defective pixel a prior pixel is substituted from an output register 34 (part of the memory 16) into the frame buffer 16 by the read pulse (control means) at the same (x, y) location of the good pixel].

[Claim 4]

Katoh teaches, "…. wherein said defect correction circuit calculates an average of image data of pixels adjacent to a subject pixel" (col. 6 lines 18-22, figure 11E).

[Claim 7]

Katoh teaches an image pickup apparatus including a display device for displaying an image signal processed by the image processing apparatus according to claim 1 (col. 5 lines 7-14).

[Claim 8]

An image pickup apparatus according to claim 7, wherein the display device is a liquid crystal display. Official Notice is taken of the fact that both the concept and advantages of providing a LCD as a display device are well known and expected in the art. It would have been obvious to have a LCD as a display device because it has a compact size and good image quality.

[Claims 10, 12, 13]

These are method claims corresponding to the apparatus claims 1 and 4 respectively. Therefore it has been analyzed and rejected based on the claim 1 and 4.

[Claim 16]

Grounds for rejecting claim 13 apply for claim16 completely. (Dividing a sum of pixel data of two pixels adjacent to a subject pixel and cutting a lowest one bit is the same as dividing the sum of pixel adjacent to each other by two i.e. taking the average of two which is the same as Claim 13).

7. Claims 3, 5, 6 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Katoh et al. (US Patent # 5,796,430) in view of Pape et al. (US Patent # 5,047,863) and in further view of Rambaldi et al. (US Patent # 6618084).

[Claim 3]

Katoh in view of Pape fails to teach "An image processing apparatus according to claim 1, wherein the second field of said memory stores information representative of a single defective pixel or the number of consecutive defective pixels and information representative of a position of the defective pixel in each line". However the above limitations are well known in the art as evidenced by Rambaldi (col. 3 lines 35-38, 49-50).

Therefore taking the combined teachings of Katoh, Pape and Rambaldi, it would have been obvious to one skilled in the art to incorporate second field of said memory storing information representative of a single defective pixel or the number of consecutive defective pixels and information representative of a position of the defective pixel in each line. Doing so

would recall the faulty pixels automatically prior to image generation as evidenced by Rambaldi (col. 3 lines 35-38).

[Claim 5]

Katoh in view of Pape fail to teach ".... an external memory, which store position data of defective pixel of the image sensor". However the above limitations are well known in the art as evidenced by Rambaldi (Col. 5 lines 33-36, figure 1)[The reference teaches that it may be desirable to include memory 26 on the chip but it may be external too].

Therefore taking the combined teachings of Pape and Rambaldi, it would have been obvious to one skilled in the art to incorporate an external memory, which store position data of defective pixel of the image sensor. Doing so would provide a memory as small as possible yet large enough to store all necessary information for correction/masking for each faulty pixel as evidenced by Rambaldi (col. 5 lines 34-36).

[Claim 6]

Pape fails to teach ".... wherein said memory is a dynamic random access memory". However the above limitations are well known in the art as evidenced by Rambaldi (col. 5 line 48). Therefore taking the combined teachings of Pape and Rambaldi as a whole, it would have been obvious to one skilled in the art to incorporate a memory, which is a dynamic random access memory. Doing so would provide a memory, which can be easily available between the size of 10 kilobits and 1 Megabit as evidenced by Rambaldi (col. 5 lines 44-45).

[Claim 11]

Claim 11 is a method claim corresponding to the apparatus claims 2 and 3. Therefore it has been analyzed and rejected based on the claims 2 and 3.

8. Claims 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Katoh et al. (US Patent # 5,796,430) in view of Pape et al. (US Patent # 5,047,863) as applied to claim 10 above and in further view of Tabei (US Patent # 5805216).

[Claim 14]

Katoh in view of Pape fail to teach ".... wherein said step calculates an average of image data of pixels adjacent to a subject pixel in a column direction ". However the above limitations are well known in the art as evidenced by Tabei (col. 2 line 1-2 figure 3D). Therefore taking the combined teachings of Katoh, Pape and Tabei, it would have been obvious to one skilled in the art to calculate an average of image data of pixels adjacent to a subject pixel in a column direction. Doing so would provide a boundary between light and dark portions the place X in which a defective pixel is present is conspicuous as evidenced by Tabei (col. 1 lines 17-20).

[Claim 15]

Katoh in view of Pape fail to teach ".... wherein said step (d) performs a weighing process in accordance with distances between pixels adjacent to a subject pixel and the subject pixel". However the above limitations are well known in the art as evidenced by Tabei (col. 6 lines 46-49 figure 12A to 12L). Therefore taking the combined teachings of Pape and Tabei, it would have been obvious to one skilled in the art to perform a weighing process in accordance with distances between pixels adjacent to a subject pixel and the subject pixel. Doing so would provide interpolation output interpolated by 12 kinds of interpolation methods as evidenced by Tabei (col. 6 lines 39-40).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yogesh K Aggarwal whose telephone number is (703) 305-0346. The examiner can normally be reached on M-F 9:00AM-5:30PM.

9. If attempts to reach the examiner by telephone are unsuccessful, the examiner's acting supervisor, Thai Tran can be reached on (703) 305-4725. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

YKA
February 1, 2005

TUAN HO
PRIMARY EXAMINER